TEXAS INSTRUMENTS
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PART I — GENERAL CONCEPTS AND TYPES OF MEMORIES

Address — Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down — (see Chip Enable Input)

Bit — Contraction of Binary digIT, i.e., a 1 or a 0; in electrical terms the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte — A word of 8 bits (see word)

Chip Enable Input — A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced power standby mode.

Chip Select Input — Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous—Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous—Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) — A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{CAS}$).

Data — Any information stored or retrieved from a memory device.

Dynamic (Read/Write) Memory (DRAM) — A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:
1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Alterable Read-Only Memory (EAROM) — A nonvolatile memory that can be field-programmed like a PROM or EPROM, but that can be electrically erased by a combination of electrical signals at its inputs.

Erasable and Programmable Read-Only Memory (EPROM)/Reprogrammable Read-Only Memory — A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase — Typically associated with EPROMs and EAROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

Field-Programmable Read-Only Memory — A read-only memory that after being manufactured, can have the data content of each memory cell altered.

Fixed Memory — A common term for ROMs, EPROMs, EAROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EAROMs is nonvolatile since their data may be easily changed.

Fully Static RAM — In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K — When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65{,}536$ bits.

Large-Scale Integration (LSI) — The description of any IC technology that enables condensing more than 100 gates onto a single chip.

Mask-Programmed Read-Only Memory — A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory — A medium capable of storage of information from which the information can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

NMOS — A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS)

Nonvolatile Memory — A memory in which the data content is maintained whether the power supply is connected or not.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

PMOS — A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory device during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program — Typically associated with EPROM memories, the procedure whereby logical 0's (or 1's) are stored into various desired locations in a previously erased device.

Program Enable — An input signal that when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) — A memory that permits access to any of its address locations in any desired sequence with similar access time to each location.
NOTE: The term as commonly used denotes a read/write memory.

Read — A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) — A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is determined by its structure and is unalterable.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) — A clock used in dynamic RAMs to control the input of the row addressed. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

Scaled-MOS (SMOS) — MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM — In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access — A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially form a single output.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMS.

Very-Large-Scale Integration (VLSI) — The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

PART II — OPERATING CONDITIONS AND CHRACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}
The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}
The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminel is given as a negative velue.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Operating Case Temperature

The case temperature (T_C) range over which the device will operate and meet the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground, V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

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Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$ of TMS4116).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

For examples of symbols of this type, see TMS4116 (e.g., t_{RLCL}).

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for RAS.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high)
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high)
$t_{h(CLCA)}$	$t_{CL\text{-}CAX}$	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	$t_{RL\text{-}CAX}$	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	$t_{RL\text{-}RAX}$	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(ACL)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

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Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

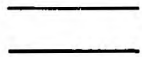
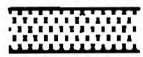
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address.

This supersedes the older form t_{PVX}.

PART III — TIMING DIAGRAMS CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

PART IV — BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key *features* such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N or P channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the *pinout* provided. Next a general *description* of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's *operation* which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Augmenting the descriptive text there appears a *logic symbol* prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 10 of this book. Following the symbol is usually a *functional block diagram*, a flowchart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Usually the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the *operating free-air temperature range*. If the device is used outside of these values, it

may be permanently destroyed or at least it would not function as intended. Next, typically, are the *recommended operating conditions,* (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), the device's operation is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings as just described can result in catastrophic failures.

The next section provides a table of *electrical characteristics over full ranges of recommended operating conditions* (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of T_A = 25°C with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing charateristics. The parameters are presented as minimum, typical (or nominal), and maximum. The *timing requirements over recommended supply voltage range and operating free-air temperature* indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The *switching characteristics over recommended supply voltage range* are device performance characteristics inherent to device operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in *timing diagrams* for each type of memory cycle (e.g., read, write, program.)

At the end of a data sheet additional *applications information* may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.